REMARKS

This application has been reviewed in light of the Office Action dated April 12, 2007. Claims 1- 26 are presented for examination, of which Claims 1 and 14 are in independent form. Claim 1 has been amended to define still more clearly what Applicant regards as their invention. Claims 1-9 and 11-13 have been amended as to matters of form; no change in scope is intended or believed effected by these changes. Claims 14-27 have been added to provide Applicants with a more complete scope of protection. Favorable reconsideration is requested.

The specification has been amended to conform the Summary of Invention section to the amended claims.

Claim 1 has been rejected based the following informality that "filed" should read --field--. Applicant has amended Claim 1 as suggested in the Office Action and, therefore, respectfully requests withdrawal of this objection.

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,084,273 (Hirota). Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirota.

As shown above, Applicant has amended independent Claim 1 in terms that more clearly define what he regard as his invention. Applicant submits that this amended independent claim and newly added Claim 14, together with the remaining claims dependent thereon, are patentably distinct from the cited prior art for at least the following reasons.

Claim 1 is directed to a photoelectric conversion device including: (1) a plurality of photoelectric conversion regions each having a first semiconductor region for accumulating electric charges that correspond to incident light; and (2) a plurality of amplifying field effect

transistors into which a signal charge from the photoelectric conversion regions is inputted. The device is characterized in that each photoelectric conversion region is surrounded by a potential barrier region, a nick region is formed in a part of the potential barrier region, and one of main electrode regions of the field effect transistors is placed adjacent to the nick region, the main electrode region having the same conductivity type as the first semiconductor region.

Among other notable features of Claim 1 is a plurality of amplifying field effect transistors into which a signal charge from the photoelectric conversion regions is inputted, wherein a nick region is formed in a part of the potential barrier region, and one of main electrode regions of the field effect transistors is placed adjacent to the nick region, the main electrode region having the same conductivity type as the first semiconductor region.

Hirota relates to a MIS device in which a threshold voltage or channel potential can be controlled in an analogue fashion. As an initial matter, Applicant respectfully submits that the Office Action improperly combines features of two separate embodiments of Hirota. For example, the Office Action (page 2) cites Figure 7 as disclosing a photoelectric conversion device. Figure 7 is a top view of CCD type solid-state image pickup device. And, Figure 8, which is a partial sectional view of Figure 7, and a partial sectional view of the CCD type solid-state image pickup device, is also cited by the Office Action as disclosing a photoelectric conversion region. The Office Action cites Figure 24 as disclosing the "amplifying field effect transistor" of Claim 1. Figure 24, however, depicts an example of an amplifying type solid-state image pickup device, not a CCD type solid-state image pickup device, and shows a completely different embodiment from that shown in Figures 7 and 8. While Figure 24 is included in the same document as Figures 7 and 8, since Figure 24 shows a different embodiment than shown in Figures 7 and 8, Applicant

submits that it is improper to combine features of Figure 24 with features of Figures 7 and 8 to establish anticipation. Accordingly, Applicants have found nothing in Hirota that would teach or suggest "a plurality of amplifying field effect transistors into which a signal charge from said photoelectric conversion regions is inputted," as recited in Claim 1.

Further, the Office Action cites Figure 8 as disclosing the "nick region" of Claim 1, citing "Fig. 8 between reference numbers 50 and 54 which acts as an overflow channel region" (Office Action, p. 3). Applicant respectfully disagrees. Reference number 50 denotes a photoelectric conversion element and reference number 54 denotes a p-type well region. The area asserted in the Office Action as constituting the overflow channel region is in fact a channel region for transferring a carrier from the photoelectric conversion element to the vertical CCD. As discussed in column 8, lines 18-23 of Hirota, an overflow drain is in a vertical over flow drain structure for sweeping out the carriers in a substrate direction. Accordingly, Applicants have found nothing in Hirota that would teach or suggest that "a nick region is formed in a part of the potential barrier region," as recited in Claim 1.

The Office Action further cites Figure 10 of Hirota as disclosing the feature of Claim 1 that one of main electrode regions of the field effect transistor is placed adjacent to the nick region. In particular, the Office Action states (page 3) that "the electrode region of FET, Fig. 10 reference number 81, lies close, or adjacent, to the nick region between the two photodiodes of reference number 86." Applicant disagrees. The item denoted by a reference numeral 86 indicated in the Office Action as being a photodiode is, in fact, a pair of diodes constituting a protective device (see column 11, lines 1-22), not a photodiode. In addition, Figure 10 merely depicts a schematic diagram of circuit connection. The protecting devices 86 are

connected at least through a switch 88 to a gate 85. As is apparent from Figure 10, only "schematic" wiring connections are shown therein. An actual semiconductor structure configuration and arrangement, wherein the two members are arranged adjacent to each other, as in the one main electrode region of the field effect transistor and the nick region, according to Claim 1, simply cannot be ascertained from the schematic diagram shown in Figure 10. Accordingly, Applicants have found nothing in Hirota that would teach or suggest "one of main electrode regions of said field effect transistors is placed adjacent to said nick region, said main electrode region having the same conductivity type as said first semiconductor region," as recited in Claim 1.

Accordingly, Applicant submits that Claim 1 is not anticipated by Hirota.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as a reference against Claim 1.

Independent Claim 14 recites features similar to those discussed above with respect to Claim 1 and therefore is also believed to be patentable over Hirota for the reasons discussed above.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request

favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

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